

App. Ser. No. 10/674,943
Reply to Office action of May 18, 2006
Reply Date: August 16, 2006

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Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

- 5 1. (Currently Amended) A method for managing performing data integrity process in an adapter, comprising:
- receiving data in a receive and/or transmit path;
- determining if a cyclic redundancy code ("CRC") mode is enabled; and
- selecting a CRC cyclic redundancy code ("CRC") mode from among plural modes
- 10 including amongst append mode, validate and keep mode, and validate and remove mode; wherein if the append mode is selected, then CRC is appended after each data block boundary.
2. (Currently Amended)The method of Claim 1, wherein adapter firmware code may be used to select a particular mode based on certain register bits ~~wherein if the append mode is selected, then CRC is appended after each data block boundary.~~
- 15 3. (Currently Amended)The method of Claim 1, wherein if the validate and keep mode is selected, then CRC accompanying any data is compared to accumulated CRC that may have been accumulated in real time while data is being sent to a host system and if an error occurs after the comparison, an interrupt is generated and data with
- 20 CRC from a storage system are sent to the host system.
4. (Currently Amended)The method of Claim 1, wherein if the validate and remove mode is selected, then CRC is first validated and then CRC is removed before data is

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sent, without involving a host system or a storage system and any errors are reported to an adapter processor out.

5. (Currently Amended) The method of Claim 1 2, wherein during an increment mode CRC seed value is incremented for each data block providing a unique CRC value for each data block.

6. (Currently Amended) The method of Claim 5, wherein ~~CRC data and~~ an optional data field ("info") and CRC are sent with a data block and the optional field is used to insert custom information. follow the actual data block.

7. (Currently Amended) A system for performing managing data integrity in receive and transmit path of an adapter process, comprising:
a processor executing firmware code CRC logic that allows firmware running on an adapter to for selecting one of plural CRC modes for implementing cyclic redundancy code ("CRC") including append mode, validate and keep mode, and validate and remove mode, wherein during append mode, a CRC engine determines CRC for each data block and CRC seed value is incremented for each data block such that each data block has a unique CRC value.

8. (Currently Amended) The system of Claim 7, wherein register bits are used for enabling and disabling the plural modes for implementing CRC. during append mode, a CRC engine determines the CRC for each data block and CRC seed value is incremented for each data block such that each data block has a unique CRC value.

9. (Currently Amended) The system of Claim 7 8, wherein during the append mode each data block is associated with ~~has a CRC value and~~ an optional field for where inserting custom information may be added ("info data").

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10. (Currently Amended) The system of Claim 7, wherein during the validate and keep mode, ~~the a~~ CRC engine compares CRC for ~~the data with accumulated~~ accumulated CRC information in real time while data is being sent to a host system and CRC is ~~sent out with data.~~

5 11. (Currently Amended) The system of Claim 10, wherein an interrupt is generated if an error occurs after the comparison and CRC received from a storage system in a receive path is sent to the host system.

12. (Currently Amended) The system of Claim 7, wherein during the validate and remove mode, ~~the CRC engine compares CRC for the data with accumulated~~ accumulated CRC information CRC is validated and then CRC information is removed before data is sent without involving a host system or a storage system out.

~~13. (Cancelled)~~

14. (Currently Amended) An adapter in a RAID controller that is coupled to a host system ~~on one side~~ and a storage media ~~on another side~~, comprising:

15 a processor executing firmware code for selecting one of plural modes for implementing cyclic redundancy code ("CRC"), CRC logic that can perform data integrity process using one of wherein the plural CRC modes include including append mode, validate and keep mode, and validate and remove mode and during the append mode, a CRC engine determines CRC for each data block and CRC seed value is incremented for each data
20 block such that each data block has a unique CRC value.

15. (Currently Amended) The system adapter of Claim 14, wherein register bits are used for enabling and disabling the plural modes for implementing CRC during append

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~~mode, a CRC engine determines the CRC for each data block and CRC seed value is incremented for each data block such that each data block has a unique CRC value.~~

16. (Currently Amended) The ~~system adapter~~ of Claim ~~14~~ 15, wherein during the append mode each data block is associated with ~~has a CRC value and an optional field which is used for inserting custom information where custom information may be added ("info data").~~
17. (Currently Amended) The ~~system adapter~~ of Claim 14, wherein during the validate and keep mode, ~~the a~~ a CRC engine compares CRC for the data with accumulated ~~accumulated~~ CRC information in real time while data is being sent to the host ~~system and CRC is sent out with data.~~
18. (Currently Amended) The ~~system adapter~~ of Claim 17, wherein an interrupt is generated if an error occurs after the comparison and CRC received from the storage system is sent to the host system.
19. (Currently Amended) The ~~system adapter~~ of Claim 14, wherein during the validate and remove mode, CRC is validated ~~the CRC engine compares CRC for the data with accumulated accumulated CRC information and CRC information is removed before data is sent~~ without involving the host system or the storage system out.
20. (Currently Amended) The ~~system adapter~~ of Claim 14, wherein the adapter is ~~CRC logic is functionally coupled to the host system via a PCI and/or PCI-X interface.~~